33.1 A 0.18μm CMOS Dual-Band Direct-Conversion DVB-H Receiver

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Digital video reception is emerging as the latest feature towards multimedia-oriented handheld devices. The broadcasting frequencies for Europe are in UHF (bands IV/V) and in the US, the 1670 to 1675MHz band that has been allocated for DVB-H operation. Additional spectrum is expected to be allocated from 1.4 to 1.5GHz (L-band) worldwide.

For integration purposes in the crowded mobile phone case, it is critical to preserve battery and minimize PCB area. To reduce power consumption, DVB-H enables DVB-T reception in a time-slicing mode by a 1:10 on/off ratio. However, typical DVB-T tuners employ super-heterodyne architectures with one or two IF stages [1] and direct sampling of the passband signal for digital quadrature down-conversion. External tracking and SAW filters are used for channel selection and image rejection. Such approaches result into increased power consumption and high number of external-components, which renders them unsuitable for integration into mobile phones. To address the need for smaller form factor, lower cost and power consumption, direct conversion TV tuners covering the UHF bands IV and V have been implemented in SiGe BiCMOS [2].

In this paper, a DVB-H tuner IC that implements a dual-band direct-conversion receiver in CMOS is presented. This tuner covers both UHF and the newly allocated bands while minimizing reference PCB area. The 64QAM-OFDM modulation and the stringent DVB-T MBRAI [3] radio-interface specifications pose significant implementation challenges, which are enhanced by the choice of architecture and process: low NF, high second- and third-order linearity are needed for a wide input-frequency range. Other issues as dc offset, I/Q mismatch, and phase noise, also require special attention as they can degrade performance for high-order modulation.

Figure 33.1.1 shows the block diagram of the chip. Fully differential structures are used to avoid noise and substrate coupling. The direct-conversion receiver consists of dual RF paths driven by off-chip baluns, covering the 470 to 890MHz and 1.4 to 1.8GHz bands, respectively. The front-end variable-gain LNA block, used in both bands, is shown in Fig. 33.1.2. The input stage is a differential cascode pair that uses integrated source inductors (Ls) for degeneration. Input matching is achieved by using external series inductors. For the UHF band, an on-chip switched capacitor bank Cb is used to maintain matching. Continuous analog gain control is achieved by current steering, controlled by a replica scheme that regulates the current of devices M3C, M3D. A feedback loop generates voltage V_{ctrl} so that the current through devices M3Rn, M3Rp is proportional to transconductance Gm, which is variable to enable programmability of the gain slope. A linear-in-dB range of 20dB is measured. To achieve high linearity and low flicker noise, both RF paths use passive mixers. A logarithmic amplifier taps the signal at the LNA output to generate a wideband linear-in-dB RSSI signal. This allows the baseband processor to backoff the LNA gain in the presence of RF interference to achieve optimum NF/linearity in order to meet blocking and intermodulation specifications.

Channel selection is performed by dual 6th-order type-I Chebyschev filters implemented by opamp-RC integrators in a leapfrog configuration. An on-chip auto-calibration loop (Fig. 33.1.3) is activated upon power-up and sets the f_o to a value from 2 to 5MHz, thus supporting the different channel bandwidths of 5 to 8MHz specified by DVB-T. During auto-calibration, a tone at the appropriate f_{-3dB}, generated on-chip, is applied at the input and is compared with the filter output using an rms detector. A digitally controlled loop adjusts the filter bandwidth by varying binary weighted capacitors Ci, until the input attenuated by 3dB equals the output.

Baseband gain control is performed by two digitally programmable gain amplifiers (PGA) before and after the channel-select filters. At the output of the first PGA, a programmable pole is used to reduce linearity requirements for the baseband filters. Since static and time-varying dc offsets can saturate the receiver output in direct conversion, both PGAs employ dc servo loops. Gain control range is 60dB with a gain step of 0.5dB. To accommodate analog gain control, the PGAs can also be controlled by an on-chip ADC.

To achieve low in-band phase noise independent of the reference crystal and channel spacing, a ΔΣ fractional-N synthesizer is used for LO generation. Fractional synthesis also allows sharing the same crystal with the mobile-phone RF transceiver while maintaining fine-tuning capability. The synthesizer employs a multi-modulus prescaler, implemented as an array of cascaded 2/3 dividers. The fractional part of the division ratio is modulated by a 3rd-order ΔΣ modulator. Two VCOs cover a range from 1.2 to 1.8GHz, using complementary cross-coupled pairs and MOS varactors in accumulation mode for tuning. A switched varactor bank provides the necessary tuning range. After a switch-channel command has been issued, a coarse tuning scheme is activated that sets the VCO control voltage to a predefined/programmable value and starts a varactor scanning sequence. Proper varactor selection is achieved by the use of a frequency detector, which determines the lowest frequency error. Quadrature LO for the UHF mixers is generated by dividing the VCO frequency by two or three, while a first-order polyphase filter is used for the L-band. As shown in Fig. 33.1.4, 0.5° of rms phase noise is typically achieved before division, which has negligible contribution to the receiver noise floor.

The chip occupies 9.7mm² (die micrograph in Fig. 33.1.7) and is implemented on a 0.18μm CMOS process. It is encapsulated in a 6×6mm² MLF 40-pin package. On-chip voltage regulators convert the external 2.7V supply to 1.8V internally and provide isolation between blocks.

Typical measured performance is summarized in Fig. 33.1.6. Figure 33.1.5 shows typical NF and gain measurements for the UHF band, both as a function of frequency and AGC voltage. NF is less than 4dB for the 470 to 702MHz range, used in GSM convergence terminals. Due to the low NF in both UHF and L-band, external LNAs [2] are avoided. Variations over a temperature range of –30 to 85°C are smaller than ±1.5 dB. The tuner is also validated with a DVB-T demodulator, showing compliance to the MBRAI specifications. An SNR of better than 30dB is measured for a –70 to –25dBm input range, limited by the digital demodulator accuracy.

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References:
[1] M. Dawkins, et al., "A Single-Chip Tuner for DVB_T," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1307-1317, Aug., 2003.
[2] P. Antoine, et al., "A Direct-Conversion Receiver for DVB-H," *ISSCC Dig. Tech. Papers*, pp. 426-427, Feb., 2005.
[3] Mobile and Portable DVB-T Radio Access Interface Specification, European Industry Association EICTA, MBRAI-02-16, Version 1.0.

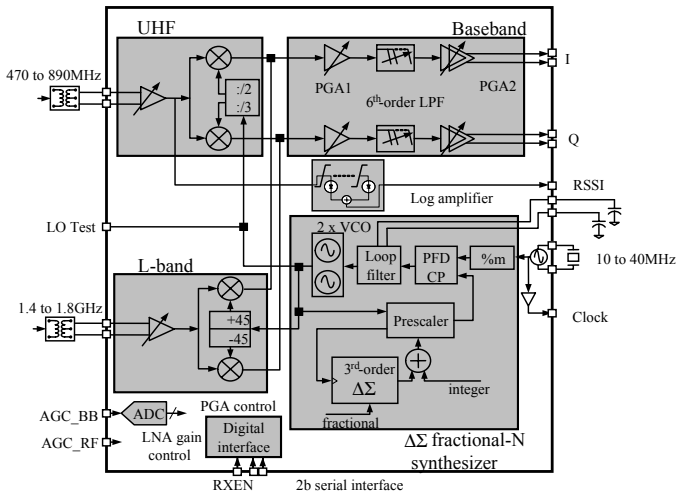

Figure 33.1.1: Tuner block diagram.

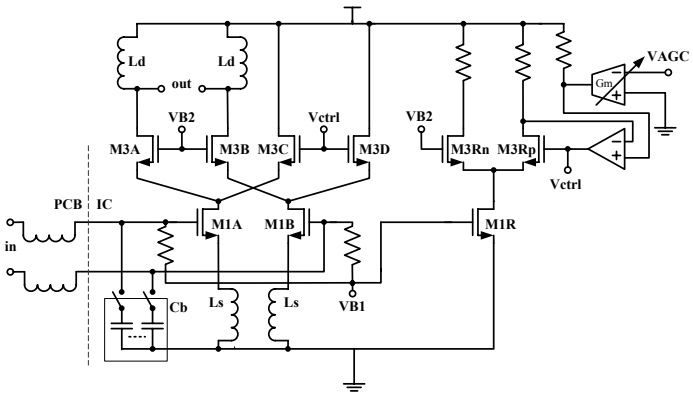

Figure 33.1.2: LNA with replica AGC.

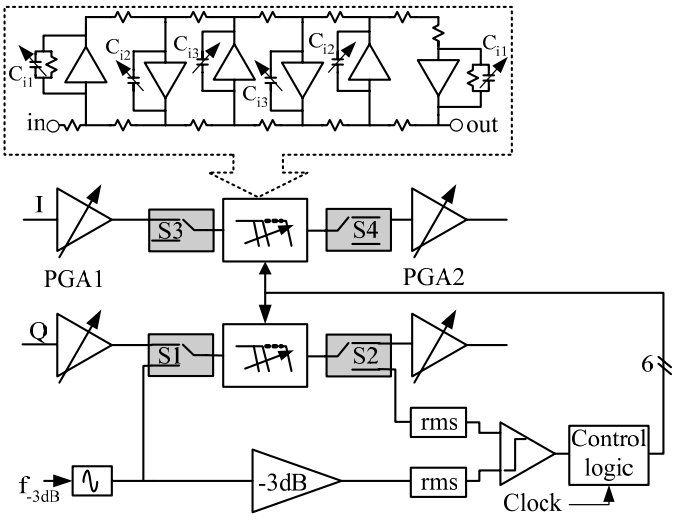

Figure 33.1.3: Baseband filter auto-calibration loop.

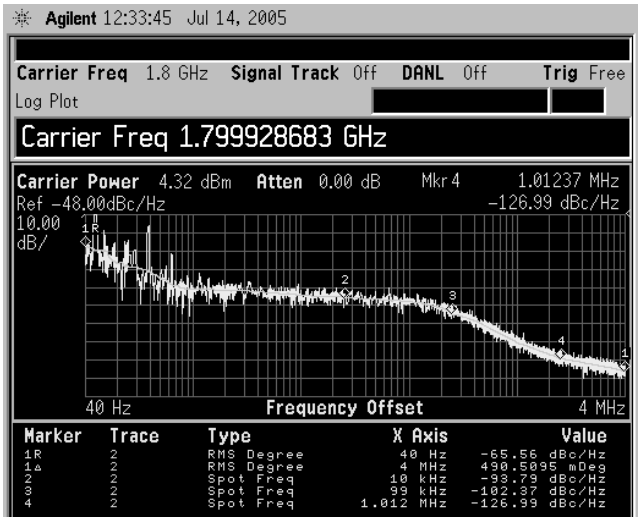

Figure 33.1.4: PLL phase noise.

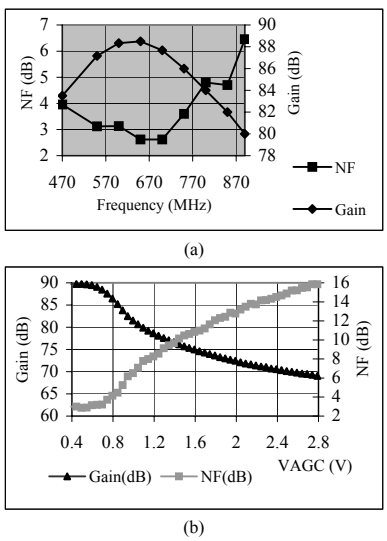

Figure 33.1.5: NF/Gain versus (a) frequency, and (b) V_{agc}.

Parameter	UHF	L-Band
Frequency range (MHz)	470-890	1400-1800
Supported RF channel BW (MHz)	4 -10	
Gain Max/Min/Step. (dB)	86/6/0.5	83/3/0.5
NF @ Max. Gain (dB) (balun included)	3.5	4
IIP3 (N+2, N+4) @ 0/6/10 dB attenuation (dBm)	-9/-3/-0.5	-5.5/-2.5/-2
IIP2 (N+2) @ 0/10/15 dB attenuation (dBm)	+21/30/34	+20/29/35
RX path attenuation at 5/8/12 MHz - 3.9 MHz BW setting (dB)	22/50/75	
LO leakage at RF input (dBm)	-88	-75
Sensitivity $2x10^{-4}$ BER (C/I =4dB), ½ QPSK mode (dBm)	-98	-96
Max. signal $2x10^{-4}$ BER (C/I =16.5dB) $^2/_3$ 64-QAM QPSK mode (dBm)	-13	-15
MBRAI L3 immunity meas./spec (dB)	43/40	-
MBRAI S2 immunity meas./spec (dB)	41/40	-
Integrated phase noise (10 Hz – 4MHz)	0.3° rms	0.5° rms
Phase noise @ 1 MHz offset (dBc/Hz)	-133	-127
Power consumption in continuous RX (mW)	295	280
Die size (mm^2)	9.7	

Figure 33.1.6: Performance summary.

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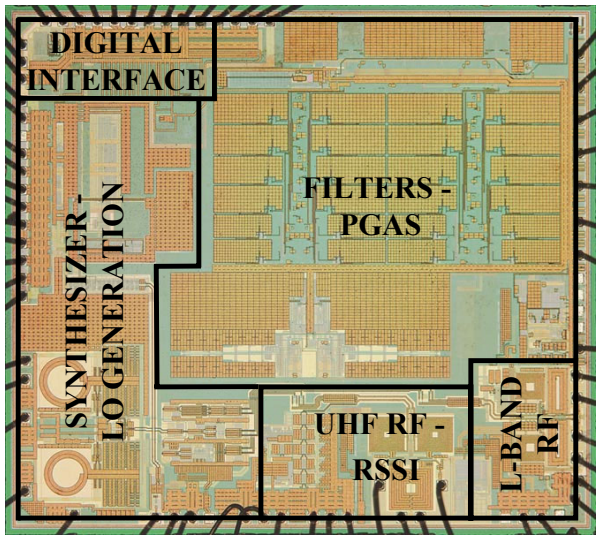

Figure 33.1.7: Die micrograph.

